Claims

[c1] A method of manufacture of a Super Steep Retrograde Well (SSRW) FET (Field Effect Transistor) device comprising:
form an SOI layer on a substrate;
thin the SOI layer to form an ultra-thin SOI layer;
form an isolation trench separating the SOI layer into N and P ground plane regions;
dope the N and P ground plane regions formed from the SOI layer with N-type and P- type dopant respectively;
form semiconductor channel regions above the N and P ground plane regions; and
form gate electrode stacks above the channel regions and the FET source and drain regions.

[c2] The method of claim 1 wherein the SOI layer is thinned by successive oxidation and stripping steps forming a thinned SOI layer.

[c3] The method of claim 2 wherein a pad oxide and a pad nitride layer are formed over the thinned SOI layer.

[c4] The method of claim 3 wherein an isolation trench is formed in the device separating the thinned SOI layer

into first and second regions.

[c5] The method of claim, 4 wherein an isolation dielectric is formed filling the isolation trench.

[c6] The method of claim 5 wherein the first and second regions are ion implanted with N-type dopant and P-type dopant to form an SOI N-well and an SOI P-well respectively.

[c7] The method of claim 6 wherein an intrinsic epitaxial layer is formed above each of the SOI N-well and the SOI P-well respectively.

[c8] The method of claim 7 wherein in situ counter doping is provided in the epitaxial layers.

[c9] The method of claim 8 wherein a liner is formed in the isolation trench prior to forming the isolation dielectric.

[c10] The method of claim 8 wherein a sacrificial layer is applied before forming the N-well and the P-well and is stripped away thereafter.

[c11] The method of claim 1 including the step of forming a diffusion retarding barrier in the surface of the N and P ground plane regions.

[c12] The method of claim 11 wherein the SOI substrate is

thinned by successive oxidation and stripping steps forming a thinned SOI layer.

[c13] The method of claim 12 wherein a pad oxide and a pad nitride layer are formed over the thinned SOI layer.

[c14] The method of claim 13 wherein an isolation trench is formed in the device separating the thinned SOI layer into first and second regions.

[c15] The method of claim 14 wherein an isolation dielectric is formed filling the isolation trench.

[c16] The method of claim 15 wherein the first and second regions are ion implanted with N-type dopant and P-type dopant to form an SOI N-well and an SOI P-well respectively.

[c17] The method of claim 15 wherein the first and second regions are ion implanted with N-type dopant and P-type dopant to form an SOI N-well and an SOI P-well respectively.

[c18] The method of claim 17 wherein in situ counter doping is provided in the intrinsic epitaxial layers.

[c19] The method of claim 18 wherein:
a liner is formed in the isolation trench prior to forming the isolation dielectric;

a sacrificial layer is applied before forming the N-well; and

the P-well and is stripped away thereafter.

[c20] A Super Steep Retrograde Well (SSRW) FET (Field Effect Transistor) device comprising:

an ultra-thin SOI layer formed on a substrate;

an isolation trench separating the SOI layer into N and P ground plane regions;

the N and P ground plane regions formed from the SOI layer doped with high doping levels of N-type and P-type dopant respectively;

semiconductor channel regions above the N and P ground plane regions;

FET source and drain regions juxtaposed with the channel regions; and

gate electrode stacks above the channel regions.